

FIGURE 1

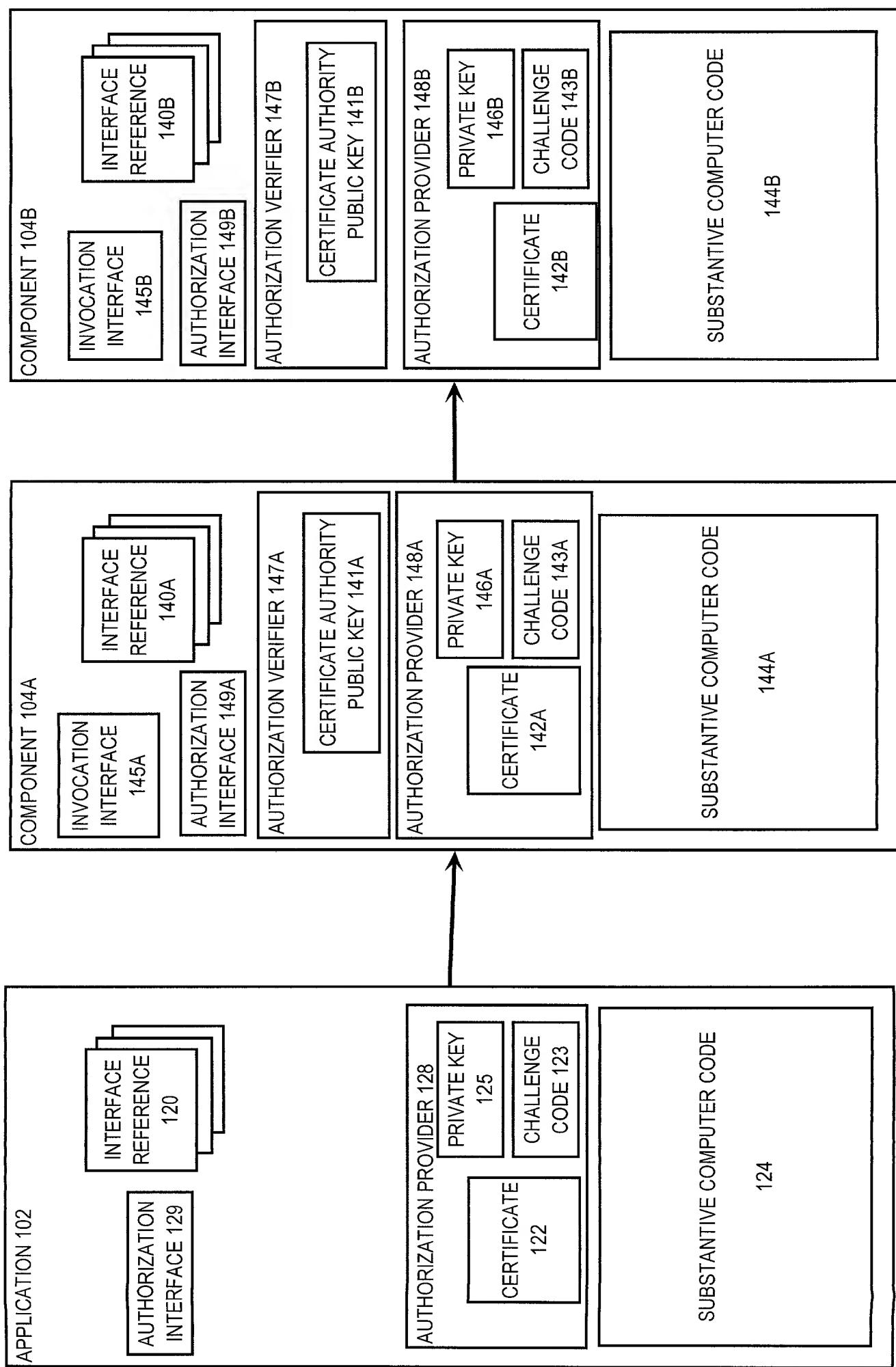


FIGURE 2

memory access times more than one clock cycle apart, and each access must be completed before the next can begin.

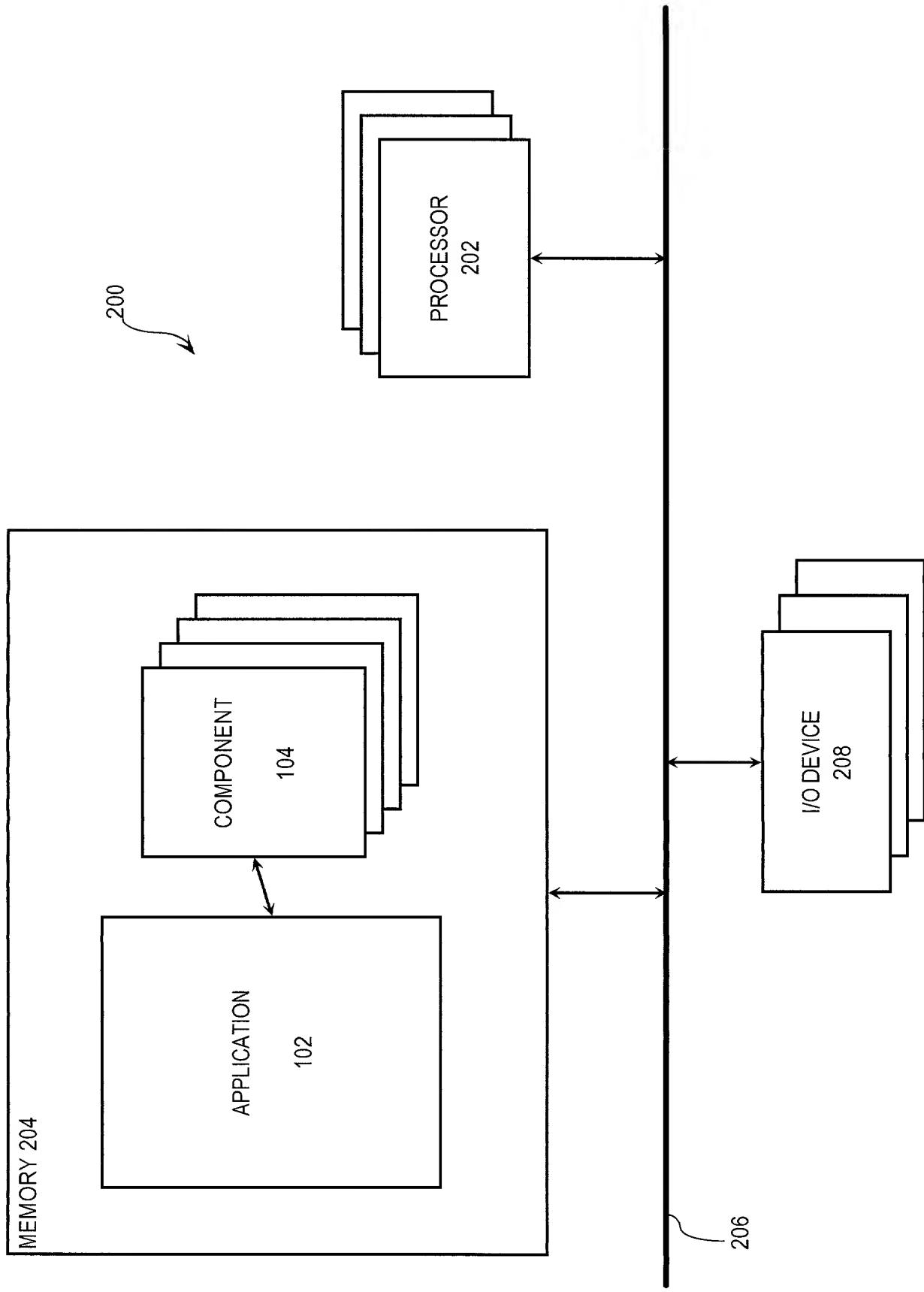
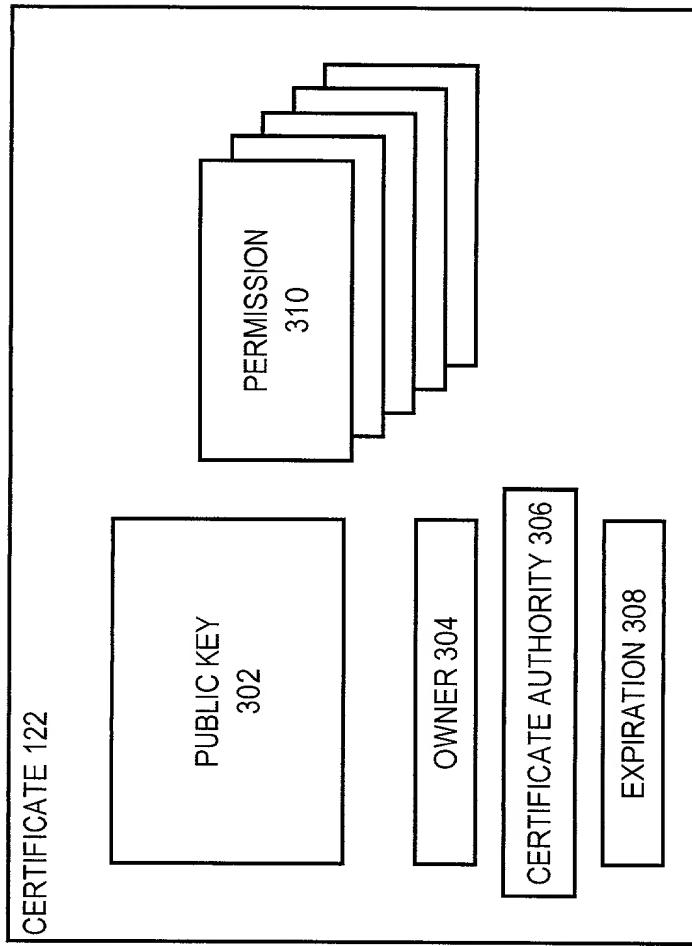


FIGURE 3



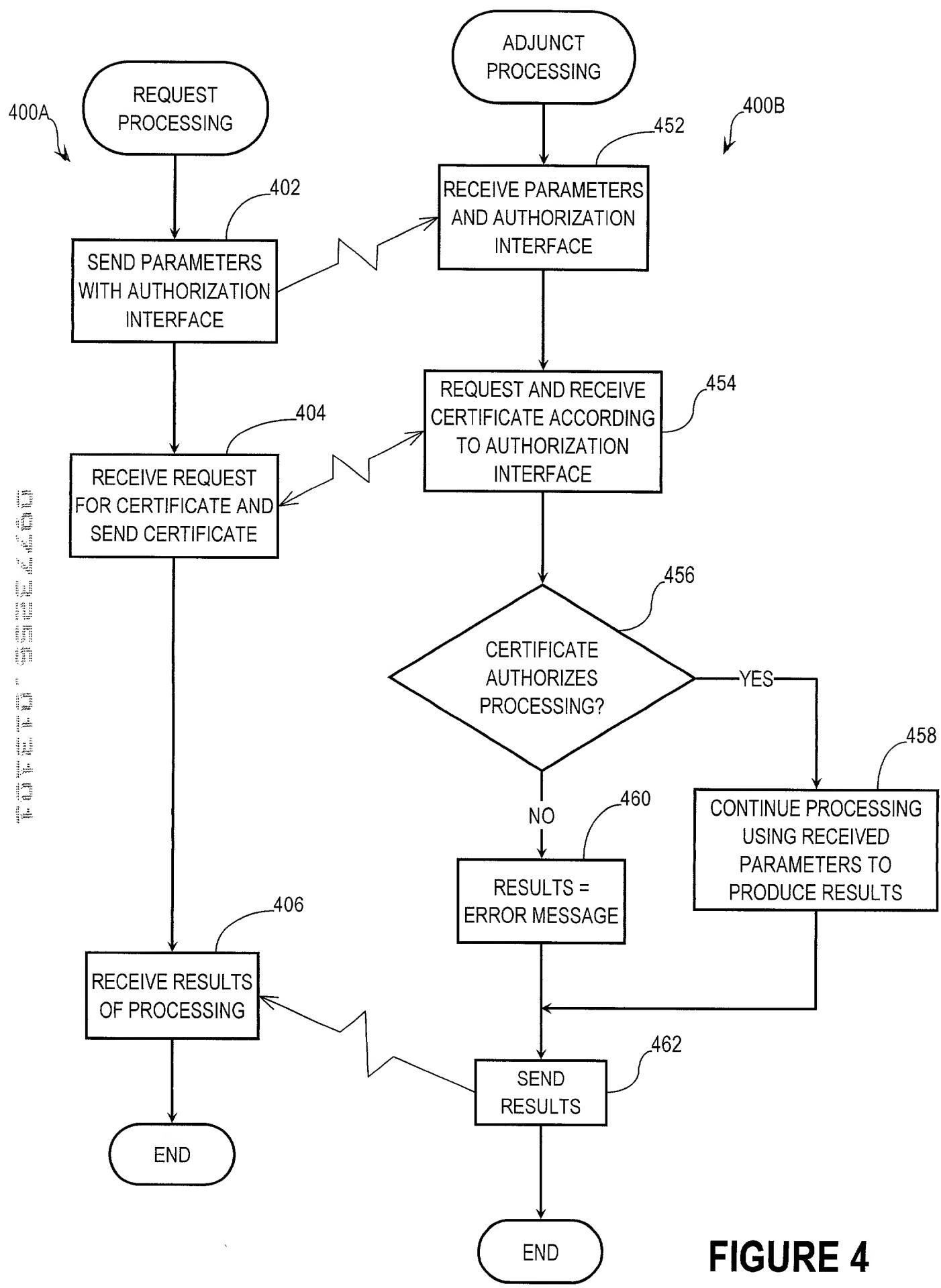
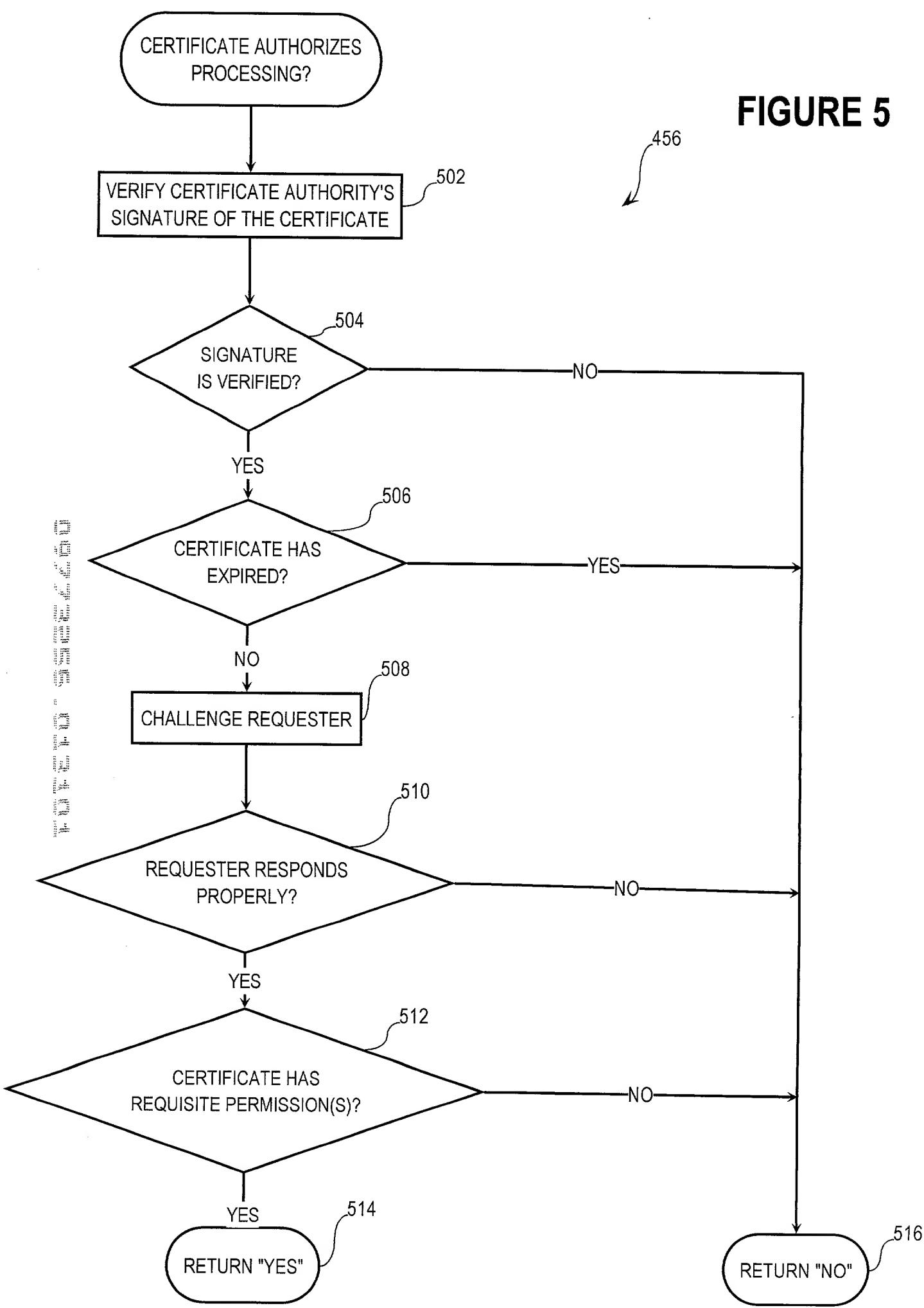


FIGURE 4

FIGURE 5



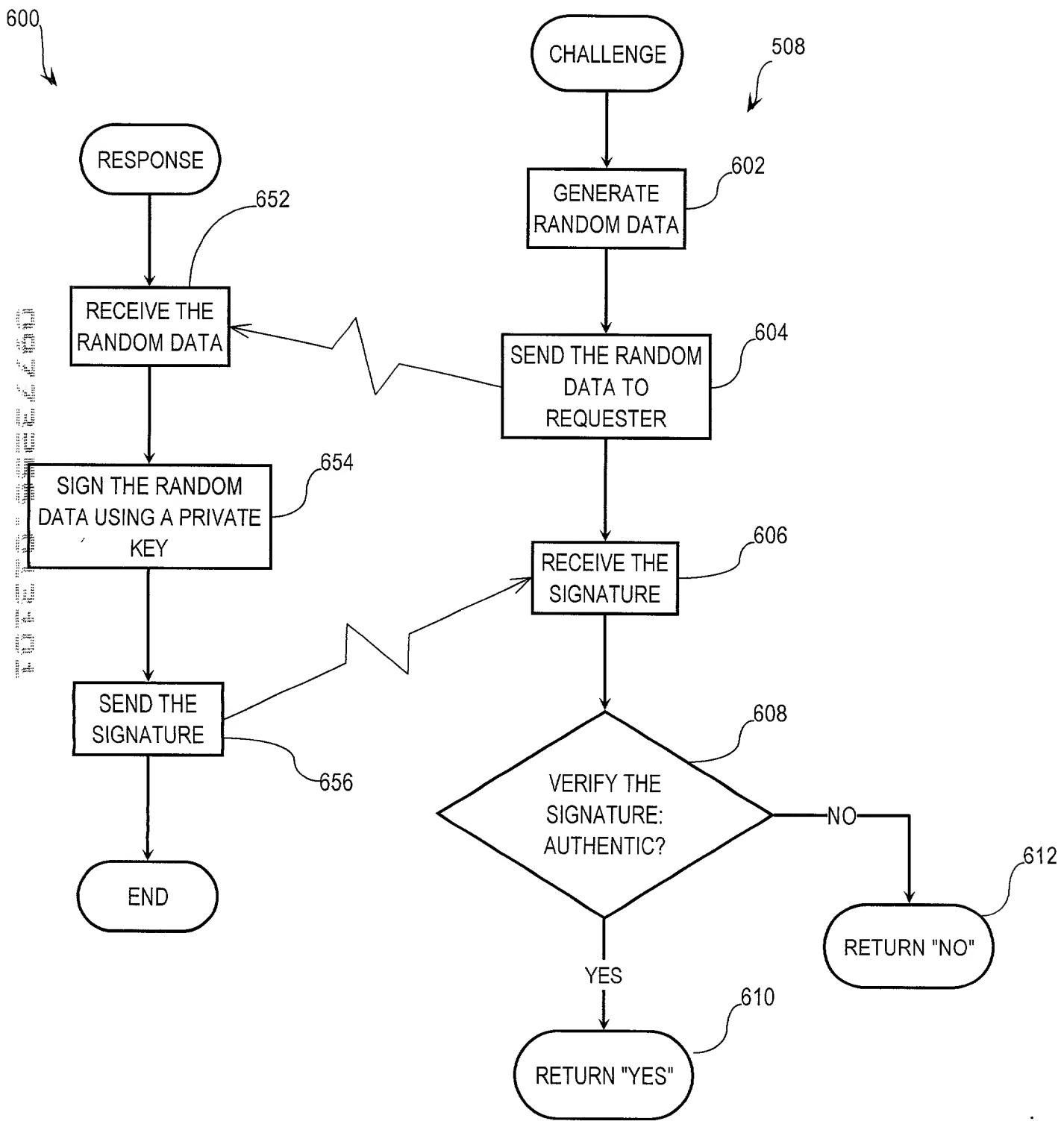


FIGURE 6A

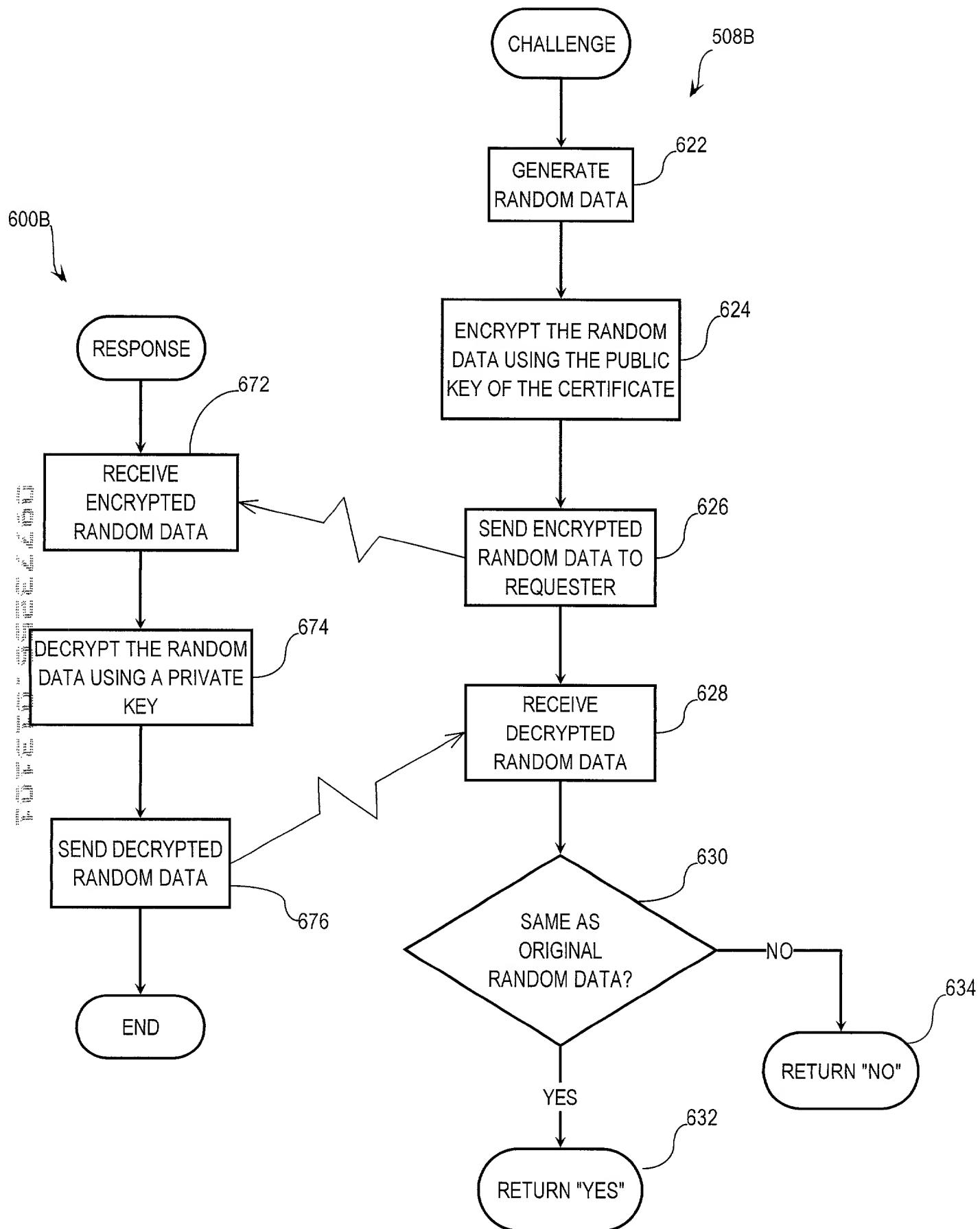


FIGURE 6B